High Frequency Mesh Network for Control and Sensor Arrays

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Abstract

This paper explores wireless mesh networking by establishing short-range telemetry links in the Industrial Scientific and Medical (ISM) frequency band of 13.56MHz and demonstrating the forwarding capabilities of a mesh network. For this purpose three transceivers are designed and built which act as nodes on the network, two of which are embedded nodes. The transceivers are designed using Phase Locked Loops (PLLs) both as a signal source and a direct Frequency Modulation (FM) demodulator.

Key words: transceivers, modulation, mesh networking, control arrays.

1. INTRODUCTION

In modern biological research facilities care must be taken not to expose experiments to too high frequency radiation since such radiation contains more energy per photon and could conceivably interfere with sensitive experiments [9]. Low power is also required for the same reasons.
It is not simple to run wires in such environments; therefore wireless solutions are preferred. It is preferable to have as few units as possible, so some form of network would be an advantage in such an application.
This paper explores the design of a low power low frequency mesh network to solve such a problem. This network may also be used as a tool to study and experiment with routing protocols and behaviours in a real environment.
The paper is organized in following manner. Section two presents review of background theory. Section three describes transceiver design. Section four gives overview of software design process.

2. THEORETICAL REVIEW

Building and testing the transceivers and networking require some knowledge of the following concepts.

2.1. Modulation

There are three types of digital modulation [3], which are summarized as follows:

In *Amplitude Shift keying/ On-off keying (ASK/OOK)* modulation scheme, the data of interest is encoded into the amplitude of he carrier wave. This scheme requires a strong signal and very selective receiver, since noise can easily cause data loss.
In *Frequency Shift Keying (FSK) and Continuous Modulated Frequency Shift Keying (CMFSK)* modulation scheme, data symbols are encoded by shifting the carrier frequency by small amounts. It does not suffer as much from noise as ASK or OOK. CMFSK is a variation of FSK where the carrier wave does not make abrupt changes in frequency, but 'slides' into the next frequency. This reduces out of band high frequency 'spurs' when the frequency shifts.
In *Phase Shift Keying (PSK)* modulation scheme, the phase of the carrier contains the data being transmitted.

This scheme gives the best performance, but is prohibitively complicated to implement.

2.2. Phase Locked Loop

Since it is difficult to generate a stable, low output impedance high frequency signal, a Phase Locked Loop (PLL) is used to multiply the frequencies using a frequency divider as shown in Figure 2.1.

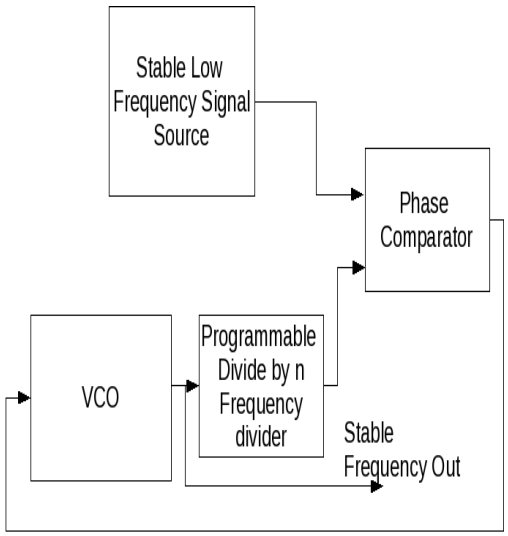

Figure 2.1 Stable signal source using a Phase Locked Loop

The heart of the phase locked loop is the phase comparator, which can take the form of an exclusive 'OR" (XOR) logic gate or JK flip-flops. The phase comparator will output a voltage that is proportional to the phase difference of the frequencies that are applied to its inputs. For comparing two frequencies, the phase comparator used should be chosen carefully. With an XOR gate comparator, the duty cycles of the incoming signals are assumed to be equal. JK flip-flop comparators do not suffer from this problem, since they are triggered on the rising edge of the incoming signals. A PLL also has a Voltage-Controlled Oscillator (VCO), normally designed to respond to the output of the comparator. If one input frequency to the comparator is a low frequency stable (for example crystal) source, and the other is the VCO signal divided by a suitable integer, and the output is feed back into the VCO, thus closing the control loop. The VCO will produce a signal as the stable source, but at a frequency *n* times the stable source. By changing *n*, the output frequency can be modified [2].

If the VCO of the PLL is stable enough and its output is fed directly into the phase comparator, and an Radio Frequency (RF) Modulated signal is fed directly into the other comparator input, the output of the phase comparator will be proportional the difference in frequency between the two signals. If the control loop is closed as in Figure 2.2, this output will represent the demodulated base band signal, and the VCO will track the input signal. A PLL can only track a signal within its locking range, and therefore the PLL behaves as a narrow band active filter. A filter placed between the comparator and the VCO may be used to adjust the characteristics of the PLL filter including its locking range and response time. This has the advantage of allowing FM demodulation without the use of mixers, tuned circuits and inter-mediate frequency stages. This greatly reduces the complexity of a receiver system.

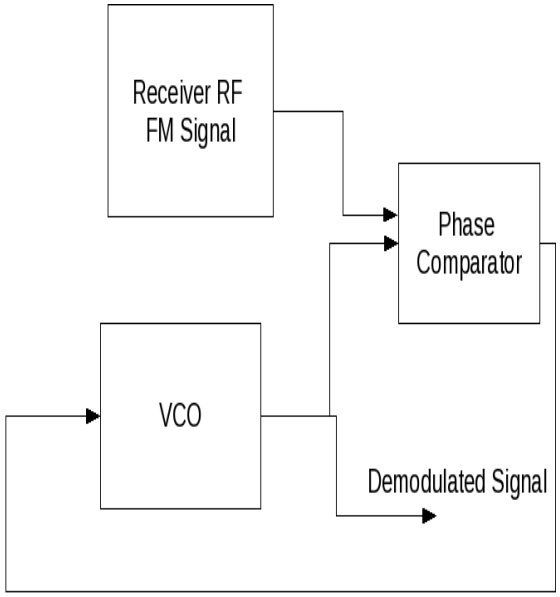

Figure 2.2 Phase Locked Loop as a direct FM demodulator

2.3. Mesh Network Routing

Mesh networking is a method of routing data and instructions between nodes on a network. It allows the network dynamically route around damaged nodes/connections, hopping between nodes until the destination

is reached. Wireless Ad-Hoc or mesh networks will allow communication beyond the range of one node, since each node will act as a router to additional nodes.
For example, in the Figure 2.3, if Node 4 fails, Node 3 may still reach Node 5, provided Nodes 1 and 2 will forward data for it. This is the 'self healing' property of Mesh Networks. When the logical structure of the network is known, each node can be pre-programmed with routing information to use optimal paths. This method only really applies to either very small networks, or networks which are not dynamic. For larger fixed networks where routing may depend on the network load, more dynamic systems are required. A common example is the Internet Protocol version 4 (IP v 4) routing used by the Internet. Ad-Hoc networks dynamically update themselves and allow the easy addition of extra nodes. Mobile Ad-Hoc networks must also deal with the additional problems caused by the mobility of the nodes. There are various protocols available with significant advantages and disadvantages [1]. In this paper only one routing algorithm is discussed. This is the optimistic 'flooding' protocol, where by each node will forward all packets to any node. It can see all nodes except the one that forwarded the packet.
The packet may only live for a specific adjustable number of hops, which should prevent routing loops. Other methods involve recording link statistics and the presence of nearby nodes in order to optimize the route.

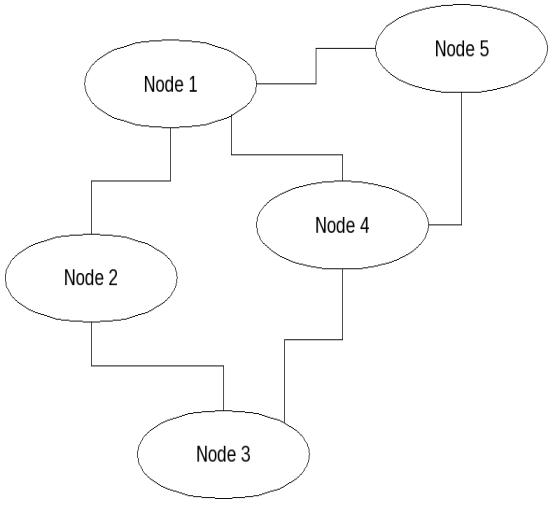

Figure 2.3 Mesh network

This introduces additional complexity and network bandwidth overhead. The protocol implemented is 'lossy' - packet delivery is not guaranteed, but is likely. The sender does not know if the packet was delivered or not. This method was chosen for experimentation and testing, but it could be expanded to include acknowledgment and resend request packets [8].

3. TRANSCEIVER DESIGN

The Transceiver is shown in Figure 3.1.

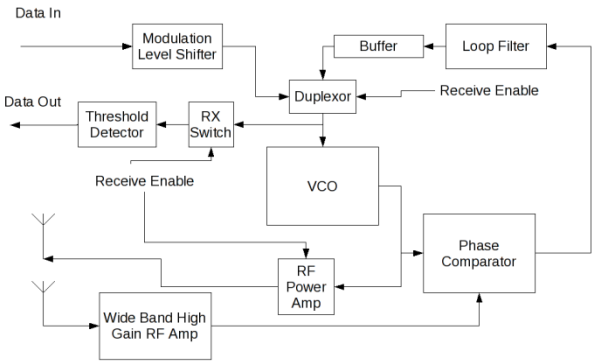

Figure 3.1: Block diagram of half-duplex FSK transceiver

The transceiver accepts Transistor-Transistor Logic (TTL) 5 V level RS-232 standard serial computer port inputs and processes them. Grounding the 'Receive' enable line enables transmission. The full schematic diagram of all modules is shown in Figure 3.2.
The heart of the transceiver module is the PLL. This is in the form of a 74HCT9046A integrated circuit (IC), (U3 on the Schematic Diagram). [7]
The IC is designed to provide both a stable VCO and high frequency operation (typically up to 17 MHz), and covers the 13.56 MHz ISM band. This IC requires an input voltage of between 3 V and 6 V. 5 V was used here, since it is standard and can also power the other components. Two resistors and one capacitor set the frequency of the internal VCO of the 74HCT9046A IC.

RV1 sets the offset frequency, while R3 sets the swing frequency; that is the range of frequencies at which the VCO may operate. When R3 is left unconnected (R3 is infinitely high) the system will only operate over a very

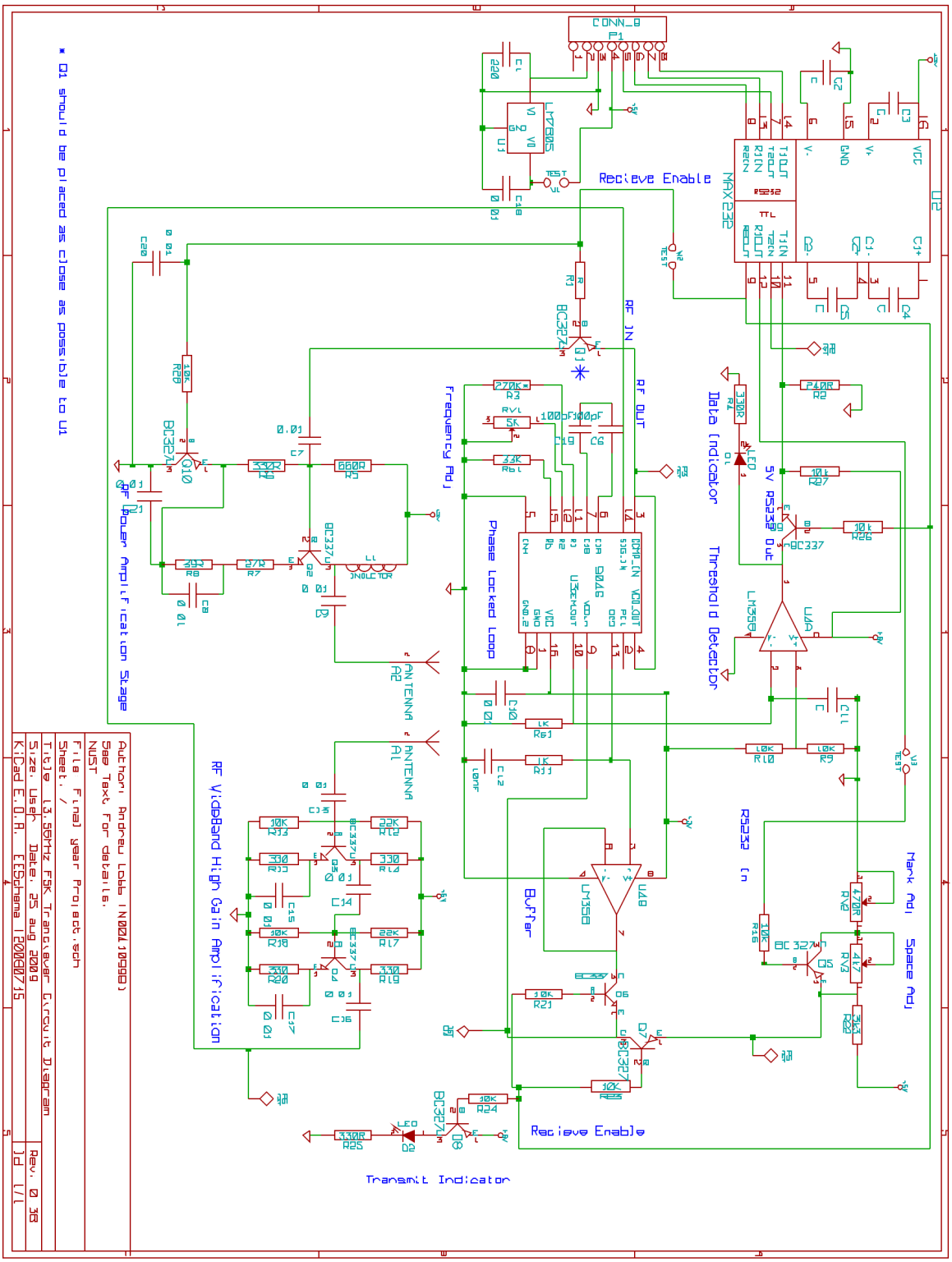

Figure 3.2. Full Schematic Diagram

narrow range of frequencies. The capacitor C6 in conjunction with RV1 sets the frequency. The VCO input voltage is only valid if it is between 1.2 V and 3.9 V. The 74HCT9046A provides a buffered output of the VCO input which may be used as a demodulated signal out. Rs1 activates that output. PC2 is the output of Phase

Comparator 2, and the inputs are COMP_IN and SIG_IN. COMP_IN is shorted to VCO_OUT directly without any dividers since it will directly demodulate Frequency Shift Keying.

The loop output current of Phase Comparator 2 (PC2) of the 74HCT9046A is controlled by Rb1. This design of a current source rather than voltage output allows the 74HCT9046A to behave as an active filter simplifying loop filter design. The other components of the filter are found on the output pin of PC2. These are R11 and C12. Rb1 creates a fictive output resistance of PC2 R'3.

The inputs of the 74HCT9046A's phase comparator are self-biasing amplifiers or buffers. These amplifiers self-bias at about 0.5 V or will accept TTL input levels. For smaller signals, capacitive coupling is required. The 0.01uF capacitor is sufficient for this purpose at these frequencies.

The transmitter must be fully disabled while the system is receiving so that the sensitive receiver does not pick up residue signal, which may interfere with the incoming signal.

To do this, two transistors Q1 and Q10 are used. Q1 is a simple switch, which greatly attenuates the input signal into the Radio Frequency (RF) power amplifier. However, to sufficiently ensure the amplifier is off it is disconnected from ground using Q10, so that it is no longer biased. Q10 must be bypassed to ground via C21 to maintain the amplifier's gain. C20 is used to pass the RF into the base of Q1 to ground and prevent it from using the tracks around Q1 to radiate and thus interfere with the receiver.

When on (that is in receive mode) Q6 allows the feedback from the phase comparator back into the 74HCT9046A VCO. When Q6 is off Q7 is on (transmit mode), Q6 allows the level shifted voltage to be input into the 74HCT9046A VCO and thus shift the transmitted frequency.

Modulation is accomplished by switching the VCO between two voltages (set by RV2 and RV3), which are switched by the state of the RS232 in line driving Q5. To invert the signal, a NPN transistor may replace Q5.

The output of the RF wideband receiver amplifier section should produce at least 0.5V peak-peak to bias the internal amplifier (74HCT9046A). This signal will have a phase difference with the locally generated signal. The phase comparator compares these signals and produces a voltage via the loop

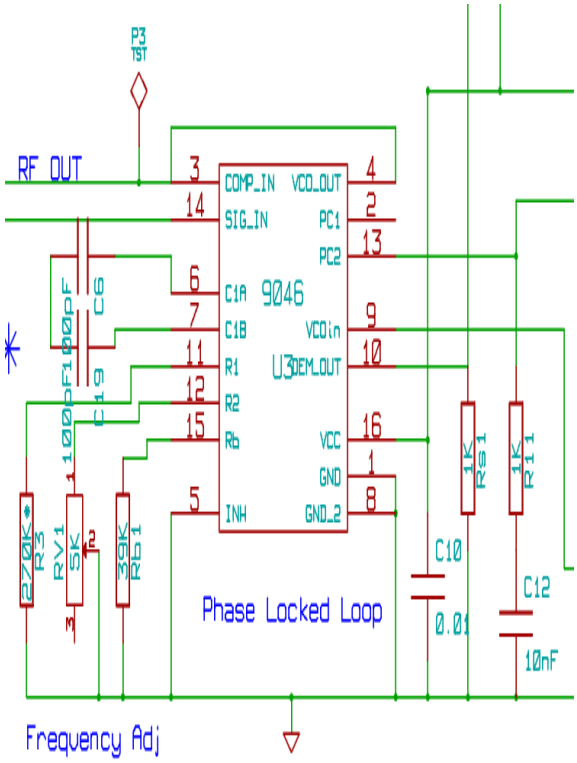

Figure 3.3: 74HCT9046A as part of the FSK transceiver.

filter. Since this voltage source has high output impedance, it cannot be directly switched by Q6 and is thus buffered by U4B (the LM358 operational amplifier IC) before being fed into the VCO input. Pin 10 of the 74HCT9046A provides a copy of this signal, which is then compared with 2.5 V by U4A to produce a RS-232 compatible signal from the incoming signal. U4B introduces noise into the system within acceptable limits.

RF power amplifier uses emitter degeneration to achieve a moderate voltage gain independent of the transistor gain. This is useful, since the input is already 5 V peak, but at low current (< 4 mA) the resistors R5 and R6 bias or open the transistor so it may work with the incoming AC signal. Capacitor C7 provides coupling from the output of the VCO. The inductor L1 has the effect of amplifying the output voltage beyond 5 V, and is a 'tuned' circuit, which helps smooth the sharp peaks of the incoming square wave into a better approximation sine wave. It also has the effect of dumping the RF through C9, and into the antenna. When Q10 is off Q2 is unbiased. This has the effect of switching off the amplifier.

Since a quarter wave antenna for this frequency is over 5m long, it is certain that any shorter antenna (like the ones used) will be mismatched, resulting in an unfavorable Standing Wave Ratio (SWR). This means that not all power produced by the power amplifier will be radiated. It is estimated (by the fact that communication distance between nodes is about 60 cm) that this is well within the legal limits and sufficient for the systems to communicate over short distances.

The gain of the receiver section is extremely high for frequencies below about 50 MHz, and thus amplifies a wide range of signals. The exact gain depends on the current gains of each individual transistor, which varies due to manufacturing process differences. The gain of this two stage amplifier was experimentally found to be sufficient for the desired purposes with a number of transistors tested. R15, R14, R19 and R20, were chosen to be 330 Ohms as this gave a good output impedance at the cost of power efficiency.

U4A (the ‘A’ side of the LM358 operational amplifier IC) acts as a threshold detector, detecting when the output of PC2 is greater or less than 2.5V. This drives a data indicator LED and also the MAX232 interface to a computer RS-232 port, or directly the pico-controller (PIC). A 240-Ohm resistor is connected between U4A's output and ground to allow it to drive TTL circuitry.

The system accepts inputs from Data Terminal Ready (DTR) and the data transmit pins of a standard serial port. The data input drives the level-shifter, while DTR set low enables transmitter and DTR set high enables the receiver. It is the job of software to detect when it may send or not. A carrier detect could be implemented later via the 74HCT9046A's PC_OUT (PC1) pin which detects when the PLL is locked and the Clear to Send (CTS) pin on a standard RS-232 serial port.

The PLL acts, as a very precise filter on the condition that its frequency can be set precisely. Therefore it is not necessary for the receiver RF section to be very selective. The PLL must have its frequency set very precisely. This requires a multi-turn precision potentiometer.

To produce the circuit schematic, Net list and Printed Circuit Board (PCB) artwork, the professional quality open source free package KiCad1 was used [6].

In order to accurately calibrate the transceivers to the 13.56 MHz ISM band, a frequency counter was required which was constructed using a PIC16F690 IC (which was later used as an embedded node).

Since timer 1 is only 16 bit, on overflow an extra 16-bit number was incremented allowing the accurate counting of frequencies. These numbers were then simply sent via RS-232 to a GNU/Linux machine running a python script, which converted the numbers into a frequency taking into account calibration data. Once calibrated to approximately the correct frequency, each receiver is tuned to a transmitter to the point where a transmitted ‘1’ causes the data indicator LED to just turn off. These systems were tested for stability by being left running in a flow of warm air overnight.

Long term stability of these transceivers may be questionable, since they use RC oscillators and have no crystal references. Tests were undertaken to establish whether all nodes were capable of communicating by causing each node in turn to transmit a ‘1’ and turn off all the other node's data indicators. Difficulties were encountered debugging and calibrating the circuits, since the circuits are fairly complex and a single dry joint can be difficult to locate.

4. SOFTWARE DESIGN

This flowchart in Figure 4.1 applies to all nodes. All nodes will follow these steps when a complete packet starting with 0x55 is received.

The PICs were programmed with PikDev, a complete integrated development environment for Microchip's PIC line of products. Python was chosen which provides a powerful and easy to use environment. Two application and user interface frameworks were considered Qt 4.1 from Nokia [4] and GTK+2 (an open source product) [5].

The Mandriva GNU/Linux operating system (2009) was chosen to run all the PC software (including PikDev, the PIC development environment and programmer, and KiCad).

Once the interface was designed, it was a simple matter to write code for all events (signals under Qt 4) that could arise. The Python Serial interface (as of August 2009) does not support an event driven system so had to be polled. In order to do this, a separate thread was created using the powerful python-threading interface. The thread sleeps when it has nothing to do and thus does not waste processor time.

A Qt 4 timer periodically checks if the serial thread has data to be processed and initiates the processing and checking of incoming packets. The PC node produces a lot of debugging information when launched from console, which may be useful in diagnosing any problems in the system.

The ‘Process Command’ box expands to a number of functions corresponding to the packet commands definition. The ‘Retransmit Packet’ box first checks if the receiver is running and introduces some random delays before transmitting.

The embedded nodes are passive nodes in this system; they do not initiate network traffic except in response to received commands. However, this may be modified in code. Embedded nodes will correctly forward traffic, decrementing the hop-count field.

All code was first tested using a PIC connected to a computer node via a MAX 232 line driver. This allows fake packets to be sent to the PIC and its response to be studied, and thus the code was tested before all the transceivers were functional. All commands and forwarding capabilities of both the PIC and PC nodes were tested in this manner. At this stage the two systems were now integrated (the node controllers - both PICs and PC software) and the hardware transceivers, and the ability of the system to forward packets and execute commands was tested.

5. CONCLUSION

This paper shows that it is possible to design a low frequency stable half duplex transceiver around a single Phase Locked Loop. However, such a system would require periodic calibration and is suboptimal outside an experimental environment. For commercial use, a system involving two PLLs, one for modulation and one for demodulation, would be more reliable over variable temperatures.

The paper also shows that it is possible to use a very simplistic optimistic flooding protocol for useful control and data capture over short ranges with small number of nodes on a wireless mesh network. Since this is a “best effort” protocol and does not guarantee packet delivery, this protocol would be inadequate for critical systems. However, the hardware allows for more complicated protocols to be implemented.

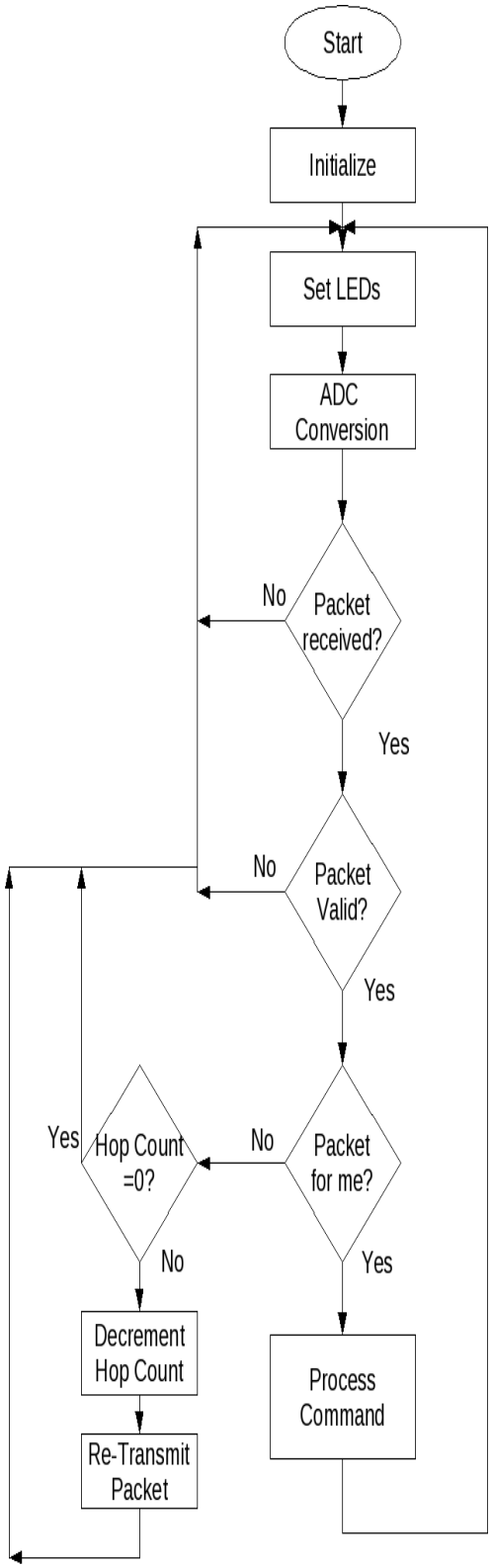

Figure 4.1: Packet received flow chart

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